**Implementation of low power D flipflop using gated clock technique**

A Project Report

Submitted in the partial fulfillment of the requirements for the award

of the degree of

# Bachelor of Technology in

Department of **ECE**

by

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**Declaration**

The Project Report entitled “ Implementation of low power D flipflop using gated clock technique“ is a record of bonafide work of M Phani gopi (170040501), Y Vasanthi (170040966), Y Deepika (170040972), submitted in partial fulfillment for the award of B.Tech in ECE to the K L University. The results embodied in this report have not been copied from any other departments/University/Institute..

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**Certificate**

This is to certify that the Project Report entitled “Implementation of low power D flipflop using gated clock technique ” is being submitted by M Phani gopi (170040501), Y Vasanthi (170040966), Y Deepika (170040972) submitted in partial fulfillment for the award of B.Tech in ECE to the K L University is a record of bonafide work carried out under our guidance and supervision.

The results embodied in this report have not been copied from any other departments/ University/Institute..

### Signature of the Supervisor

Dr N Siddaiah

### Signature of the HOD Signature of the External Examine

**Acknowledgment**

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**Abstract**

In this work, we address the issue of leakage power that arises with the device channel length scaling. We present a circuit technique to mitigate the leakage currents of MOSFET through controlling the clock my modifying clock circuit with respected gated clock. CMOS inverter designed using the proposed technique results in improvement in static and total power dissipation respectively compared with its conventional design. The simulation results of D flipflop and PISO circuit designed using the same technique indicates improvement in the total power compared with their corresponding conventional designs. Memory element designed using the proposed technique is analyzed, and corresponding simulation results are reported.

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**Introduction**

Scaling of CMOS technology improved the speed nevertheless the leakage currents are leftover as an adverse effect. The problem has taken a serious turn as the scaling extends into ultra-deep-submicron (UDSM) region. These unsolicited leakage currents should be minimized for the smooth functioning of the circuit.Project aims in reducing average power consumption of D flip flop and it will be further implemented on parallel in serial out memory element.

**Literature survey**

The technique to be used to reduce power consumption is gated clock technique which is flexible on any of software as well as provide good reliability to circuit in terms of power and number of transistors. Mentor graphics is the software used with 130nm technology.

Initially the method is implemented of single D flip flop and later be implemented of PISO memory element

In this work, an analysis of speed and power dissipation performance for existing clock-gated flip-flops has been done to figure out the trade-offs imposed by the inclusion of the clock-gating circuitry, and to make a proposal avoiding those disadvantages. Project deals with some previous work done on regards of clock-gated flip-flops, and presents modified schemes to improve the speed and power consumption performance exhibited by previous proposal. And also presents the proposed clock-gated pulse-triggered flip-flop, and explains the key features for having a better performance for this circuit. It shows the simulations results carried out to compare the performance of our proposal and former ones.

The Results below shows simulation graph and indicates amount of power consumed for each of the model. Here all four models of D flip flop and memory elements are shown with average power values and results clearly shows that modified circuit consumes less power even if the transistor count of un modified circuit is less than that of modified circuit. The reason behind less power consumption is due to the fact that the circuit will be in off state whenever there is no operation

**Theoretical analysis**

**Need for Low Power Circuit Design**

The increasing prominence of portable systems and the need to limit power consumption (and hence, heat dissipation) in very-high density ULSI chips have led to rapid and innovative developments in low-power design during the recent years. The driving forces behind these developments are portable applications requiring low power dissipation and high throughput, such as notebook computers, portable communication devices and personal digital assistants (PDAs).In most of these cases, the requirements of low power consumption must be met along with equally demanding goals of high chip density and high throughput. Hence, low-power design of digital integrated circuits has emerged as a very active and rapidly developing field of CMOS design. The limited battery lifetime typically imposes very strict demands on the overall power consumption of the portable system. Although new rechargeable battery types such as NickelMetal Hydride (NiMH) are being developed with higher energy capacity than that of the conventional Nickel-Cadmium (NiCd) batteries, revolutionary increase of the energy capacity is not expected in the near future. The energy density (amount of energy stored per unit weight) offered by the new battery technologies (e.g., NiMH) is about 30 Watt-hour/pound, which is still low in view of the expanding applications of portable systems. Therefore, reducing the power dissipation of integrated circuits through design improvements is a major challenge in portable systems design. The need for low-power design is also becoming a major issue in high-performance digital systems, such as microprocessors, digital signal processors (DSPs) and other applications. Increasing chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. If the clock frequency of the chip increases then the power dissipation of the chip, and thus, the temperature, increase linearly. Since the dissipated heat must be removed effectively to keep the chip temperature at an acceptable level, the cost of packaging, cooling and heat removal becomes a significant factor. Several high-performance microprocessor chips designed in the early 1990s (e.g., Intel Pentium, DEC Alpha, PowerPC) operate at clock frequencies in the range of 100 to 300 MHz, and their typical power consumption is between 20 and 50 W. ULSI reliability is yet another concern which points to the need for low-power design. There is a close correlation between the peak power dissipation of digital circuits and reliability problems such as electro migration and hot-carrier induced device degradation. Also, the thermal stress caused by heat dissipation on chip is a major reliability concern. Consequently, the reduction of power consumption is also crucial for reliability enhancement. The methodologies which are used to achieve low power consumption in digital systems span a wide range, from device/process level to algorithm level. Device characteristics (e.g., threshold voltage), device geometries and interconnect properties are significant factors in lowering the power consumption. Circuit-level measures such as the proper choice of circuit design styles, reduction of the voltage swing and clocking strategies can be used to reduce power dissipation at the transistor level. Architecture-level measures include smart power management of various system blocks, utilization of pipelining and parallelism, and design of bus structures. Finally, the power consumed by the system can be reduced by a proper selection of the data processing algorithms, specifically to minimize the number of switching events for a given task.

Scaling of CMOS technology improved the speed nevertheless the leakage currents are leftover as an adverse effect. The problem has taken a serious turn as the scaling extends into ultra-deep-submicron (UDSM) region. These unsolicited leakage currents should be minimized for the smooth functioning of the circuit.Project aims in reducing average power consumption of D flip flop and it will be further implemented on parallel in serial out memory element.

**D Flip flop**

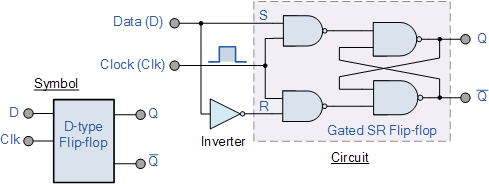
The D-type flip-flop is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic level. One of the main disadvantages of the basic SR NAND Gate Bistable circuit is that the indeterminate input condition of SET = “0” and RESET = “0” is forbidden.

This state will force both outputs to be at logic “1”, over-riding the feedback latching action and whichever input goes to logic level “1” first will lose control, while the other input still at logic “0” controls the resulting state of the latch.

But in order to prevent this from happening an inverter can be connected between the “SET” and the “RESET” inputs to produce another type of flip flop circuit known as a Data Latch*,*Delay flip flop*,*D-type Bistable*,*D-type Flip Flopor just simply a **D Flip Flop** as it is more generally called.

The **D Flip Flop** is by far the most important of the clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at the same time. The D-type flip flop are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (Data) input.

Then this single data input, labelled “D” and is used in place of the “Set” signal, and the inverter is used to generate the complementary “Reset” input thereby making a level-sensitive D-type flip-flop from a level-sensitive SR-latch as now S = D and R = not D as shown.



We remember that a simple SR flip-flop requires two inputs, one to “SET” the output and one to “RESET” the output. By connecting an inverter (NOT gate) to the SR flip-flop we can “SET” and “RESET” the flip-flop using just one input as now the two input signals are complements of each other. This complement avoids the ambiguity inherent in the SR latch when both inputs are LOW, since that state is no longer possible.

Thus this single input is called the “DATA” input. If this data input is held HIGH the flip flop would be “SET” and when it is LOW the flip flop would change and become “RESET”. However, this would be rather pointless since the output of the flip flop would always change on every pulse applied to this data input.

To avoid this an additional input called the “CLOCK” or “ENABLE” input is used to isolate the data input from the flip flop’s latching circuitry after the desired data has been stored. The effect is that D input condition is only copied to the output Q when the clock input is active. This then forms the basis of another sequential device called a **D Flip Flop**.

The “D flip flop” will store and output whatever logic level is applied to its data terminal so long as the clock input is HIGH. Once the clock input goes LOW the “set” and “reset” inputs of the flip-flop are both held at logic level “1” so it will not change state and store whatever data was present on its output before the clock transition occurred. In other words the output is “latched” at either logic “0” or logic “1”.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Clk | D | Q | Q | Description |
| ↓ » 0 | X | Q | Q | Memory no change |
| ↑ » 1 | 0 | 0 | 1 | Reset Q » 0 |
| ↑ » 1 | 1 | 1 | 0 | Set Q » 1 |

**flip flop for low power VLSI applications**

Technology and speed have always progressed hand in hand, from low scale integration to large and very large scale integration and from megahertz (MHz) to gigahertz (GHz). Similarly the system requirements are also rising up with this continuous advancement in process of technology and speed of operation. It is known that low power flip-flops are crucial for the design of low-power digital systems. In this paper we analyse the details of various flip-flop design and optimization of various parameters. We have review and study of lowest power flip-flops and comparing their performances in the areas of Cost, Power consumption, Delay are also important

As the feature size of CMOS technology process shrinks according to Moore’s Law, designers are able to integrate more transistors onto the same integrated circuit. As the number of transistors increase, it will result into increased switching and hence more power dissipation. Heat is one of the important packaging challenges in this period; being one of the main reasons for highlighting the need of low power design methodologies and practices. Another reason for taking up low power research is the reliability of the integrated circuit. In addition to this, The clock system, which consists of the clock distribution network and timing elements (flip-flops and latches), is one of the most power consuming components in a VLSI system. It accounts for 30% to 60% of the total power dissipation in a system. As a result, reducing the power consumption of flip-flops will have a major impact on the total power consumption of the circuit.

**Conventional flip flop**

A novel explicit pulse triggered flip flop is designed. This flip flop consist of a pulse generator and a transmission gate.The proposed design adopts a signal feedthrough technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X [9], [10]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during “1” to “0” data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feedthrough. This scheme actually improves the “0” to “1” delay and thus reduces the disparity between the rise time and the fall time delays.

**Principles Of FF Operations**

When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q\_fdbk assume complementary signal levels and the pull-down path of node X is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a “0” to “1” data transition occurs, node X is discharged to turn on transistor MP2, which then pulls node Q high.this corresponds to the worst case timing of the FF operations as the discharging path conducts only for a pulse duration. However, with the signal feedthrough scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. when a “1” to “0” data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of “0” to “1” data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

CMOS is a good technology for low-power as gates only dissipate energy when they are switching. However, many gates switch because they are connected to the clock, not because they have new inputs to process. As a result, a synchronous circuit wastes power when particular blocks of logic are not utilized. The largest gate is the clock driver, which must distribute a clock signal evenly to all parts of a circuit, and it must switch all the time to provide the timing reference even if only a small part of the chip has something useful to do.

As an alternative approach, asynchronous circuits are inherently data driven and are only active when performing useful work. Parts of an asynchronous circuit that receive less data will automatically operate at a lower average frequency. Asynchronous circuits are larger than synchronous circuits because additional logic is required for synchronization of the design.

An emerging newer approach, still in the early phase of commercial use is based on implementation of reversible logic or adiabatic logic. The fundamental premise of the reversible logic is to reduce power consumption by not erasing information. With conventional logic implementations, a bit of information is erased every time a logic operation is performed. The new approach using reversible logic operations that do not erase information can dissipate arbitrarily little heat.

# **Power Reduction Techniques for Ultra-Low-Power Solutions**

The consumer demand for greater functionality and higher performance, but also for lower costs adds significant pressure on System-on-Chip (SoC) manufacturers. The continuing advances in process technology, and ability to design highly complex SoCs does not come without a cost. So the next generation of processes surely brings about the next generation of challenges.

With ever increasing System-on-Chip (SoC) complexity, energy consumption has become the most critical constraint for today’s integrated circuit (IC) design. Consequently, a lot of effort is spent in designing for low-power dissipation. Power consumption has become a primary constraint in design, along with performance, clock frequency and die size. Lower power can be achieved only by designing at all levels of abstraction: from architectural design to intellectual property (IP) component selection and physical implementation. Energy reduction techniques can also be applied at all levels of the system.

Designers should use components that deploy the latest developments in low-power technology. The most effective power savings can be achieved by making the right choices early on during the system and architectural level of abstraction. In addition to using power-conscious hardware design techniques, it is important to save power through careful design of the operating system and application programs.

**Design Abstraction Levels**

In general, power reduction can be implemented at different levels of design abstraction: system, architectural, gate, circuit and the technology level. At the system level, inactive modules may be turned off to save power. At the architectural level, parallel hardware may be used to reduce global interconnect and allow a reduction in supply voltage without degrading system throughput. Clock gating is commonly used at the gate level. A variety of design techniques can be used at the circuit level to reduce both dynamic and static power.

For a given design specification, designers have many choices to make at different levels of abstraction. Based on particular design constraints (such as power, performance, cost), the designer must select a particular algorithm, architecture and determine various parameters such as supply voltage and clock frequency. This multi-dimensional design space offers a wide range of possible trade-offs. Properties of a design are most influential at the highest levels of abstraction; therefore, the most effective design decisions derive from choosing and optimizing architectures and algorithms at those levels.

However, it becomes a challenge to predict the consequences and effectiveness of design decisions made at the higher levels of abstraction because implementation details can only be accurately modeled or estimated at the technological level. Therefore, it is important to use IP components such as embedded memories and logic libraries that offer flexibility in selecting different design and power saving techniques.

**Sources of Power Dissipation**

The sources of energy consumption on a CMOS chip can be classified as static and dynamic power dissipation. The dominant component of energy consumption in CMOS is dynamic power consumption caused by the actual effort of the circuit to switch. A first order approximation of the dynamic power consumption of CMOS circuitry is given by the formula:

P = C \* V2 \* f

where P is the power, C is the effective switch capacitance, V is the supply voltage, and f is the frequency of operation. The power dissipation arises from the charging and discharging of the circuit node capacitances found on the output of every logic gate. Every low-to-high logic transition in a digital circuit incurs a change of voltage, drawing energy from the power supply.

A designer at the technological and architectural level can try to minimize the variables in these equations to minimize the overall energy consumption. However, power minimization is often a complex process of trade-offs between speed, area, and power consumption.

Static energy consumption is caused by short circuit currents, bias, and leakage currents. During the transition on the input of a CMOS gate both p and n channel devices may conduct simultaneously, briefly establishing a short from the supply voltage to ground. While statically-biased gates are usually found in a few specialized circuits such as PLAs, their use has been dramatically reduced. Leakage current is becoming the dominant component of static energy consumption. Until recently, it was seen as a secondary order effect; however, the total amount of static power consumption doubles with every new process node.

Energy consumption in CMOS circuitry is proportional to capacitance; therefore, a technique that can be used to reduce energy consumption is to minimize the capacitance. This can be achieved at the architectural level of design as well as at the logic and physical implementation level.

Connections to external components, such as external memory, typically have much greater capacitance than connections to on-chip resources. As a result, accessing external memory can increase energy consumption. Consequently, a way to reduce capacitance is to reduce external accesses and optimize the system by using on-chip resources such as caches and registers. In addition, use of fewer external outputs and infrequent switching will result in dynamic power savings.

Routing capacitance is the main cause of the limitation in clock frequency. Circuits that are able to run faster can do so because of a lower routing capacitance. Consequently, they dissipate less power at a given clock frequency. So, energy reduction can be achieved by optimizing the clock frequency of the design, even if the resulting performance is far in excess of the requirements.

**Power Reduction Techniques**

One of the most effective ways of reducing power at the technological level is to reduce the supply voltage, because the power consumption drops quadratically with the supply voltage. However, lowering supply voltage results in reduction of performance; therefore, any such voltage reduction must be balanced against any performance drop. To compensate and maintain the same throughput, extra hardware can be added. This can only be successful to the point where the additional circuitry does not diminish the savings.

Modern integrated circuits requiring longer battery life are implemented with variable clock frequency and operating voltage controlled by the operating system. The variable voltage and frequency represent a trade-off between delay and power consumption. Reducing clock frequency alone doesn't necessarily reduce power, since the system must run longer to do the same work.

A novel explicit pulse triggered flip flop is designed. This flip flop consist of a pulse generator and a transmission gate.The proposed design adopts a signal feedthrough technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X [9], [10]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during “1” to “0” data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feedthrough. This scheme actually improves the “0” to “1” delay and thus reduces the disparity between the rise time and the fall time delays.

As voltage is reduced, the delay of the circuit increases. A common approach to power reduction is to first increase the performance of the module (by adding parallel hardware for example) and then reduce the voltage as much as possible so that the required performance is still reached. However, these techniques often translate to larger area requirements, resulting in a new trade-off between area and power.

The CMOS power consumption is proportional to the clock frequency — dynamically turning off the clock to unused logic or peripherals is an obvious way to reduce power consumption. Control can be done at the hardware level or it can be managed by the operating system of the application. For example, some systems and hardware devices have sleep or idle modes. Typically, in these modes, the clocks to most of the sections are turned off to reduce power consumption. In sleep mode, the device is not working where a wake-up event rouses the device from sleep mode. Devices may require different amounts of time to wake-up from different sleep modes.

**Alternative Approaches**

The alternative approach to reducing wasteful activity is applying an asynchronous design methodology. CMOS is a good technology for low-power as gates only dissipate energy when they are switching. However, many gates switch because they are connected to the clock, not because they have new inputs to process. As a result, a synchronous circuit wastes power when particular blocks of logic are not utilized. The largest gate is the clock driver, which must distribute a clock signal evenly to all parts of a circuit, and it must switch all the time to provide the timing reference even if only a small part of the chip has something useful to do.

As an alternative approach, asynchronous circuits are inherently data driven and are only active when performing useful work. Parts of an asynchronous circuit that receive less data will automatically operate at a lower average frequency. Asynchronous circuits are larger than synchronous circuits because additional logic is required for synchronization of the design.

An emerging newer approach, still in the early phase of commercial use is based on implementation of reversible logic or adiabatic logic. The fundamental premise of the reversible logic is to reduce power consumption by not erasing information. With conventional logic implementations, a bit of information is erased every time a logic operation is performed. The new approach using reversible logic operations that do not erase information can dissipate arbitrarily little heat.

Contemporary place and route systems can perform automatic transistor resizing. The optimal gate sizing is essential for achieving both performance and power consumption goals. The better drive capability of larger transistors improves the circuit performance. This also reduces the short-circuit power because of shorter rise and fall times. However, oversized transistors result in an unnecessary waste of dynamic and static power. For that reason, it is essential to use a logic library with a large number of output drive strengths.

**Conclusion**

Growing complexity and increasing operating clock frequencies have outpaced the scaling of process geometries and supply voltages in SoC designs, thus producing an effective rise in power dissipation by these devices and pushing heat removal and power distribution to the forefront of issues confronting the advance of microelectronics. Today system-level power management has become pervasive in the semiconductor industry and power-consumption conscious system developers are now looking for a wide range of semiconductor IP platform solutions that will eliminate the gaps between low-power and high-performance requirements.

**FirstPass-Silicon Characterization Program**

Virage Logic’s FirstPass-Silicon Characterization Program provides a dedicated lab where semiconductor IP is tested and characterized under various voltage and temperature conditions. This ensures the delivery of silicon proven, manufacturable semiconductor IP across a wide range of foundries and process technologies. In addition to design correlation, the feedback from silicon is used for reliability studies and product improvements. Virage Logic’s FirstPass-Silicon Characterization Program eliminates the potential risks associated with using third-party IP and customers are ensured the delivery of high yielding, manufacturable and reliable semiconductor IP.

**Foundry Support**

Virage Logic develops and markets embedded memories, logic libraries and I/O libraries on all major pure-play contract foundries and optimizes them for numerous Integrated Device Manufacturer (IDM) in-house foundries. Virage Logic delivers solutions that provide the most optimum performance, the smallest possible area and the lowest power achievable for every foundry. Virage Logic’s memory, logic and I/O products are available in processes from 0.35µ to 90nm geometries.

**EDA Views**

Virage Logic has developed a closed-loop verification methodology that ensures all front-end and back-end views are accurate and optimized for key components of ASIC design flows from leading EDA companies including Cadence, Magma Design Automation, Mentor Graphics, Synopsys and others.

**About Virage Logic**

Virage Logic is a leading provider of best-in-class semiconductor intellectual property (IP) platforms based on memory, logic, and I/Os that are silicon-proven and production ready. Virage Logic meets market demands for cost reduction, while improving performance and reliability for integrated device manufacturers (IDMs), fabless and foundry companies focused on the consumer, communications and networking, handheld and portable, and computer and graphics markets. The company is headquartered in Fremont, California with sales, support and research and development offices worldwide.

**Software used - Mentor Graphics :**

Mentor Graphics is a technology leader in electronic design automation (EDA), providing software and hardware design solutions that enable companies to develop better electronic products faster and more cost-effectively. Mentor graphics offers innovative products and solutions that help engineers overcome the design challenges they face in the increasingly complex worlds of board and chip design. Mentor Graphics has the broadest industry portfolio of best-in-class products and is the only EDA company with an embedded software solution. Mentor graphics provide effective design and development in various fields like, Electronic Design Automation, electronic systems, automotive, CAE simulation and testing, Embedded system.

**Clock gating technique**

Clock gating is a well-known technique for reducing the power consumption of a synchronous digital system. In this article, we’ll discuss the basic concepts of clock gating.

Register File: An Example Application for Clock Gating

In this section, we’ll examine the operation of a register file as an example application where clock gating can significantly reduce the power consumption. A processor utilizes a register file as a fast temporary storage device.

##### 1.jpg

As shown in Figure 1, the heart of a register file is an array of D-type flip-flops (DFFs). We can envision these DFFs as a two-dimensional array. In Figure 1, there are n rows where each row consists of eight DFFs. The FFs in each row are placed inside a dashed box. We can write an eight-bit data word to, or read an eight-bit data word from, any of these n rows.

To perform the write/read operation, we need to specify the target row. This is achieved by specifying an address for each row of the register file. Moreover, since only one operation, either write or read, is allowed at a time, we need another input to specify whether we are writing to or reading from the file. In Figure 1, the one-bit input wr\_en, which stands for write enable, determines the operation type. When wr\_en is high, we are writing; otherwise, the register file is in read mode.

In write mode (wr\_en=1), the “decoder” block will choose one of the rows based on the value of the write address w\_addr. This will set the select input of the target row multiplexer to one and w\_data, which is the write data, will be passed to the row input. At the upcoming rising edge of the clock, w\_data will be stored in the DFFs of the selected row.

To perform the read operation, we again need to select the target row. This is achieved using a multiplexer at the output of the register file. The select input of this multiplexer is connected to r\_addr which specifies the read address. Moreover, during the read operation, we have to return the data stored in each row back to its input so that the content of the registers doesn’t change unintentionally at the clock edge. In other words, when in read mode, we are specifying the current value of a register as its next value. To this end, a two-input multiplexer is placed at the input of each row. During the read operation, the select input of all these multiplexers is logic low and, hence, the content of each DFF is returned to its input.

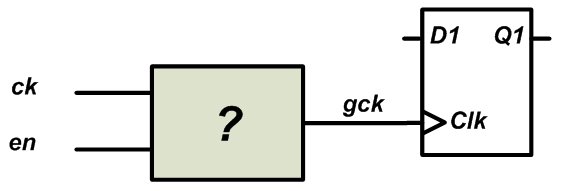
### Read Mode Wastes Power

Read mode is not efficient from power consumption point of view. In this mode, the content of the register file doesn’t need to be updated; however, with each clock tick, we are updating the registers with their current value. This requires applying the clock signal to a large number of DFFs. Remember that the [clock input of each FF introduces some parasitic capacitance](https://www.allaboutcircuits.com/textbook/digital/chpt-3/cmos-gate-circuitry/) (let’s call this capacitance CdffCdff). Hence, for an n-by-8 array of DFFs, the clock input will see a parasitic capacitance of

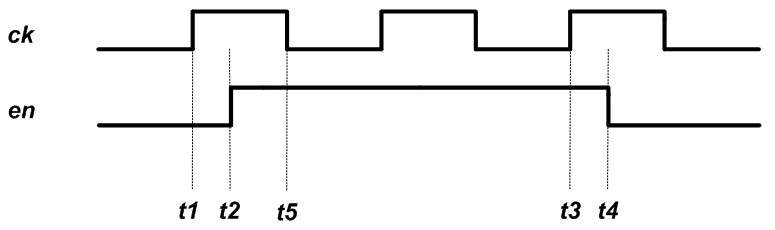
Cpar=n×8×CdffCpar=n×8×Cdff

Here, we have ignored the parasitic capacitance of the clock distribution network itself, though this capacitance can be significant.

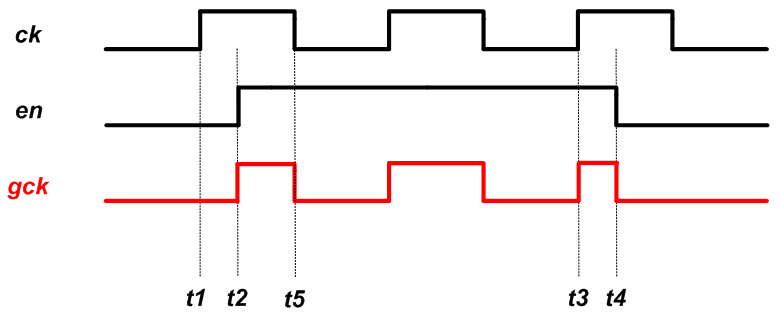
Each time the clock signal switches from zero to one, the clock distribution circuitry charges CparCpar to logic high. This requires drawing current from the power supply; the higher CparCpar becomes, the more current we will need. How can we avoid charging this capacitance? During the read operation, the content of the register file must not change. The approach shown above ensures that the register values will not change, but we can achieve the same thing by simply switching off the clock signal. This technique, called clock gating, can significantly reduce power consumption. However, it can lead to serious problems too. Assume that we have decided to use a gated clock for the DFF shown in Figure 2. The main clock is ck and we have an enable signal, en, which determines when the DFF should operate (in the register file example, the write enable signal, wr\_en, can be used for clock gating purposes). When en is logic high, the gated clock, gck, will be equal to ck. This is the basic concept of clock gating. But, what if en is logic low? Should gck be high or low in this case? What circuit should we use instead of the box labeled with the question mark in Figure 2?



##### Since the DFF shown in Figure 2 is sensitive to the positive edge of the clock, we assume that the en signal too comes from devices that change state at the rising edge of the clock. For example, in Figure 3, the clock signal, ck, goes from low to high at t=t1; some time later, the en signal transitions to high at t=t2. The time difference t2-t1 corresponds to the delay of the circuitry that produces the en signal. As an example, we can assume that a particular output of a [finite state machine](https://www.allaboutcircuits.com/technical-articles/implementing-a-finite-state-machine-in-vhdl/) (FSM) generates the en signal. In this case, t2-t1 will correspond to the delay of the FFs that store this particular state of the FSM plus the delay of the combinational circuit that generates the en signal from the FSM state (we are assuming that the system is synchronous and the FSM changes state with ck). Hence, the transitions of en will occur some time after the rising edge of ck.



Let’s use the above example waveforms to find a circuit that can generate an appropriate gated clock, gck, for Figure 2. From t2 to t4, the en signal is high and gck must be equal to ck. What if en is logic low? Should gck be high or low in this case? First, we assume that, for en=0, gck is set to low. Then, we’ll get the red waveform shown in Figure 4. To generate this waveform, we replace the unknown circuit of Figure 2 with an AND gate as shown in Figure 5.

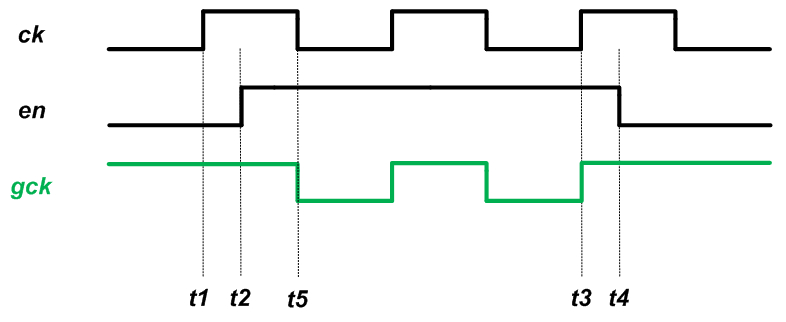


##### 5.jpg

There are a few problems with this clock gating. First, do we really need a rising edge for gck at t=t2? One may think that the rising edge of gck at t=t2 is the delayed version of the rising edge of ck at t=t1; however, note that, at t=t1, we have en=0 and, hence, the clock edge of ck must not reach the FF. Thus, this gating arrangement produces an undesired rising-edge transition.

Another issue is that the pulse width from t2 to t5 is shorter than that of ck. A very short pulse can cause the DFF to malfunction. There is a third problem with this technique that we’ll discuss soon.

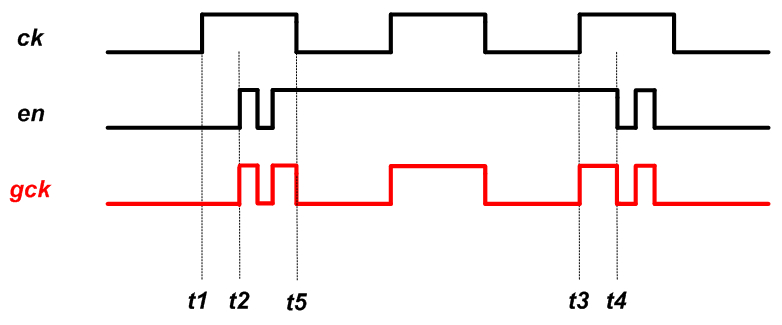
Let’s examine the next possibility: when en is logic high, the gated clock, gck, will be equal to ck but, for en=0, gck will be set to high. Then, we’ll get the green waveform shown in Figure 6. To generate this waveform, we can use the circuit shown in Figure 7.



##### 7.jpg

As you can see, unlike the gck of Figure 4, the gck generated in Figure 6 doesn’t have the rising edge at t=t2. With the circuit of Figure 7, a rising edge is presented to the DFF only when en is high and a rising edge occurs on ck. Moreover, the generated pulse width cannot be shorter than that of the original clock.

The clock gating of Figure 7 has another important advantage over that of Figure 5, namely, it is more resilient to glitches on the en signal. As discussed above, we assume that our synchronous system triggers changes at the rising edge of the clock. Also, we assume that the logic that generates the en signal has a delay that is less than half the period of ck. This means that en will start changing state right after the rising edge of ck (at t=t1) and will reach its final value before the next falling edge of ck, i.e., before t=t5. However, before reaching its final value, the en signal can have glitches. Let’s see what happens if we use clock gating with an enable signal that experiences undesired transitions. Figure 8 shows the example waveforms for the circuit of 5.



As you can see, the glitches on en are directly passed to the gated clock. These glitches can cause gck to have multiple rising edges for a single positive edge of ck, in some cases this can be disastrous, for example, assume that this gated clock is applied to a counter. The output of the counter will depend on the number of the rising edges of gck which, in turn, depends on the en glitches. Moreover, the main goal of using clock gating was to reduce the power consumption by eliminating unnecessary transitions of ck but, now, we are making the situation even worse because the en glitches are also introducing additional undesired transitions in the clock path. Examining the circuit of Figure 7, we observe that this circuit is resilient to glitches that happen during the high state of ck:

##### 9.jpg

The above discussion shows that for a synchronous system in which the logic is driven by the rising edge of the clock, we should use the OR-based circuit of Figure 7. However, for a synchronous system in which the logic is driven by the falling edge of the clock, we should use an AND gate to generate the gated clock (see Section 1.10.5 of [this book](https://www.amazon.com/Digital-Systems-Design-Electrical-Engineering/dp/053495099X) for details).

### Clock Gating in FPGAs

Clock gating is a common technique used to reduce power consumption in the context of application-specific integrated circuit (ASIC) design. However, in FPGAs, we normally avoid gating the clock. This is mainly due to the fact that, in an FPGA, dedicated nets and buffers are utilized to appropriately route the clock signal to different parts of the chip. Clock gating can interfere with the clock distribution network, for example, by forcing the clock signal to go through a general-purpose lookup table. If clock gating is utilized in FPGAs, it’s up to the designer to check that the synthesized circuits are safe.

However, power optimization software packages can be used to apply the concepts of clock gating in order to reduce the power consumption of the circuit. For example, Xilinx has an option called “[Intelligent Clock Gating](https://www.xilinx.com/support/documentation/white_papers/wp370_Intelligent_Clock_Gating.pdf)” which uses the clock enable pin in a slice to neutralize superfluous switching activity. The technique is different from the classic clock gating discussed in this article because Intelligent Clock Gating doesn’t actually create new clocks. Instead, Xilinx’s technique uses clock enable pins of slices to disable registers that don’t contribute to the circuit’s operation for a given clock cycle. You can find details about this technique in this [application note](https://china.xilinx.com/support/documentation/application_notes/xapp790-7-series-clock-gating.pdf).

* Classic clock gating can significantly reduce power consumption. This can be done, for example, by switching off the clock signal for DFFs that don’t change state.
* For a synchronous system in which the logic is driven by the rising edge of the clock, we should use an OR gate to generate the gated clock. In this case, we’ll have correct timing along with resilience to glitches.
* For a synchronous system in which the logic is driven by the falling edge of the clock, we should use an AND gate to generate the gated clock.
* In FPGAs, classic clock gating is discouraged because it can lead to unexpected or undesired functionality.

**Survey**

As the feature size of CMOS technology process increases the more switching and the more power dissipated in the form of heat or radiation. Heat is one of the most important packaging challenges in this era; it is one of the main drivers of low power design methodologies and practices. Another mover of low power research is the reliability of the integrated circuit. More switching implies higher average current is flowing and therefore the probability of reliability issues occurring rises. The most important prime mover of low power research and design is our convergence to a mobile society. With this profound trend continuing, and without a matching trend in battery life expectancy, the more low power issues will have to be addressed. This entails that low power tools and methodologies have to be developed and adhered to. The current trends will eventually mandate low power design automation on a very large scale to match the trends of power consumption of today’s integrated chips. Most of the current designs are synchronous which implies that flip-flops and latches are involved in one way or another in the data and control paths. One of the challenges of low power methodologies for synchronous systems is the power consumption of these flip-flops and latches. It is important to save power in these flip-flops and latches without compromising state integrity or performance. Several researchers have worked on low power flip-flop design, but they are mostly focused on one or a few types of flip-flops or applications. The need for comparing different designs and approaches is the main motivation during survey. The main trade-offs of any flip-flop are very important for a design engineer when designing a circuit or for a tool that automates the process of design.

**Survey of different available flipflops:**

Flip-flops can be classified in several ways: dynamic vs. static, square-wave vs. pulsed, conditional vs. non-conditional, and also according to the logic style used.We consider different flip-flop circuits to gain real insights in these different classifications. They were generally built using cadence schematic capture Virtuoso tool and sized for minimum possible size to function correctly. The following is a short description of the flip-flop circuits.Power PC master-slave latch is one of the fastest classical structures and its main advantage is the short direct path and low power feedback. The large load on the clock will greatly affect the total power consumption of the flip-flop. This flip-flop is called the transmission gate flip-flop, it has a fully static master–slave structure, which is constructed by cascading two identical pass gate latches and provides a short clock to output latency. It does have a bad data to output latency because of the positive setup time. Sensitivity to clock signal slopes and data feed through is another concern when using it. standard dynamic C2 MOS master-slave latch has shown good low power features, like small clock load and low power feedback. The hybrid–latch flip-flop (HLFF) that is one of the fastest flip-flop structures. It is robust to clock signal slopes, but it does have a positive hold time. This is very suitable for high performance systems. The semi-dynamic flip-flop (SDFF) is one of the fastest structures. It does have a large clock load and large effective pre-charge capacitance which result in a slightly high power consumption. This is still best suited for high performance designs, though its power consumption is moderate. edge-triggered latch (ETL) is very fast but its differential structure along with the pre-charge cause a slight increase in power consumption. The modified cascade voltage switch logic (CVSL) flip-flop has one of its advantages is using fewer transistors than other flip-flops. No floating nodes but still only one of the output nodes of the input stage can be fully pulled to a weak “0” which might cause more power consumption. The modified sense amplifier flip-flop (SAFF) incorporates a pre-charge sense amplifier and a set and reset latch to hold the data. SAFF’s latency is a little higher than other flip-flops due to the delay of one output from the other in the output stage. This drawback is avoided in this modified design, where it supports fully symmetric output transitions. The explicitly pulsed flip-flop (EPFF) consists of a two stage dynamic structure, which has its effect on the power consumption. Noise immunity is another concern with any dynamic design style.The single transistor clocked EPFF uses two static latch stages sharing one clock transistor.The conditionally pre-charged flip-flop (CPFF) due to the notoriety of dynamic circuits for high power consumption, the CPFF adds conditional logic for the gate to pre-charge; otherwise the pre-charge step is skipped saving its power. It does come with a cost of higher setup time for the conditional logic to evaluate and give an output to the rest of the flip-flop. In the alternative CPFF the transparency to input glitches is avoided by using an inverter which prevents the propagation of any glitches during the transparency period.

**Theoritical Analysis**

In the past, during the desktop PC era, VLSI design’s primary goal was to optimize the speed of the real-time computational functions such as gaming, video compressing, and graphics. Due to that, we now have semiconductor ICs that can integrate various graphical processing units and signal processing modules that have the ability to fulfill our demands for entertainment and computation. While these design efforts have achieved the real-time computation power, they have not addressed the increasing need of portable devices such as mobile phones that are capable enough to carry the same complex operations without consuming as much power.

The rising demand for portable and even wearable electronic devices for communication, computing, and entertainment has necessitated longer battery life, lower power consumption, and lesser device weight. Considering this, there seems a need to develop a solution that can make use of low voltage and low power design techniques. Now that power consumption is also considered as an important criterion in VLSI design, the design space might get expanded, thus adding to the complexity of the already significant tasks. In order to create an ideal solution for this problem, ‘[low power design](https://www.einfochips.com/services/silicon-engineering/physical-design-dft/)’ has to be considered as a crucial factor.

Today’s consumers want a device that is packed with all the state-of-the-art features at a reasonably low price. They need mobile devices and applications that deliver the same level of efficiency as their non-mobile counterparts, without compromising the battery life. If we analyze the top features that consumers ask for in a smartphone, about 70% of users want a long talk and standby time. They want sleeker mobile phones, which might require high levels of silicon integration used for advanced processes; however, these processes have higher power dissipation, which further results in increased temperature.

### Minimizing Power Dissipation with Low Power Design

Several measures can be taken by [VLSI companies to reduce the power dissipation](https://www.einfochips.com/resources/publications/efficiently-estimate-and-optimize-leakage-in-socs/). Some of the ways in which low power design can be implemented are discussed below:

#### Reduce supply voltage

Reducing voltage can prove to be an effective way to reduce power consumption. Without needing any special technologies or circuits, a factor of two reductions in the supply voltage can result in a factor of four reductions in the power consumption. However, the performance is also reduced by reducing the supply voltage, which can be avoided by scaling down the threshold voltage.

#### Physical capacitance

The dynamic power consumption of the circuit directly depends on the physical capacitance being switched. So, over and above reducing voltage, reducing capacitance can be another way to achieve lower dissipation.

#### Design process

Low power VLSI can be achieved by optimization at numerous levels of the design process starting from the system and algorithmic levels to circuit and layout levels.

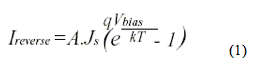
Rapid development of such portable systems as laptops, PDAs, digital wrist watches, implantable pacemakers and [cell phones](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=cell%20phones&x=&y=) require low power consumption and high density ICs. As a result there is a surge of innovative development in low power device and design techniques. In most cases, the requirements for low power consumption must meet the equally demanding goals of high [chip](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=chip&x=&y=) density and high throughput circuits. Hence, low power digital design and digital ICs are very active fields of research and development. In this cutting-edge technology, reduction in power dissipation is a critical task, especially as the size of transistors is scaled down to increase [transistor](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=transistor&x=&y=) density over the silicon chip. Reduction in power dissipation is also an important objective in the design of digital circuits. This paper discusses the techniques of designing with low power [CMOS](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=CMOS&x=&y=) circuits.

The total power dissipation in a CMOS [circuit](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=circuit&x=&y=) can be expressed as the sum of three main components:

1. Static power dissipation (due to leakage current when the circuit is idle)
2. Dynamic power dissipation (when the circuit is switching)
3. Short-circuit power dissipation during switching of transistors

Static power dissipation  
When a CMOS circuit is in an idle state there is still some static power dissipation–a result of leakage current through nominally off transistors. Both nMOS and pMOS transistors used in CMOS logic gates have finite reverse leakage and sub-threshold currents. In a silicon chip there are millions of transistors and the overall power dissipation due to leakage current is comparable to dynamic power dissipation. The values of leakage and sub-threshold currents depend upon [processing](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=processing&x=&y=) parameters. Consider an nMOS transistor shown in Figure 1.

The main leakage current component in nMOS is the reverse-biased diode structure in which the n+ bar forms the n-junction and p-substrate forming the p-junction of the diode. The magnitude of this leakage current is given by equation-1.



Where Vbias is the voltage across junction,  
A is the junction area,  
q is the charge of electron,  
k is the Boltzmann's constant (1.3807X10e-23 J/K) and  
T is the operating temperature.

Diode formation due to MOS structure is inherent, which results in leakage current. This current increases with increases in temperature. Millions of transistors are fabricated on a silicon chip and every transistor constitutes the leakage current. The sum of all leakage currents then becomes significant.

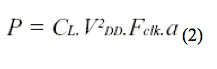
Another component of leakage current in CMOS circuits is the sub-threshold current, which is due to career diffusion between the source- and drain-region when the transistor is in weak inversion. Sub-threshold current becomes significant when the voltage at gate with respect to source is slightly less or equal to the threshold voltage (Vt) of the MOSFET. At this stage the power dissipation due to sub-threshold leakage current can become comparable to dynamic (or switching) power dissipation. The magnitude of the sub-threshold current also depends upon certain device parameters. The causes of leakage current are complex and far removed from the realm of [architecture](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=architecture&x=&y=) of digital circuits. Yet the static power dissipation is comparable to dynamic power dissipation.

Out of various techniques to minimize the leakage and sub-threshold currents to minimize static power dissipation one can use a variable threshold CMOS (VTCMOS) circuit, which is easier to achieve and is further discussed here. The basic principle of a VTMOS circuit is to keep the substrate separate from source and apply different voltage to it with respect to source (See Figure-2).

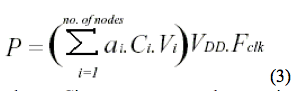
Dynamic power dissipation  
Dynamic power dissipation occurs when the MOS transistor switches to charge and discharge the output load capacitance at a particular node at operating frequency. Depicted the Figure 3 is a CMOS inverter with [output](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=output&x=&y=) load capacitance CL.

During the charge-up phase, the output node [voltage](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=voltage&x=&y=) typically makes a full transition from 0 to VDD and an amount of energy from the power supply is dissipated as heat in the conducting pMOS transistor. During the load capacitance discharge phase no power is drawn from the [power supply](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=power%20supply&x=&y=) only the energy stored (during the charge-up phase) in the output capacitance is dissipated as heat in conducting the nMOS transistor. With small static power, the charging and discharging of output node capacitance consumes most of the power in CMOS circuits.

The dynamic power dissipation at a particular output node is then given by:



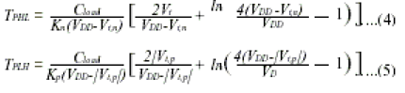
Where CL is the total output node capacitance, VDD is the supply voltage at which the output capacitance charges, Fclk is the operating frequency and is the node transition activity factor, which is the effective number of power-consuming voltage transitions experienced per [clock](http://www.mobilehandsetdesignline.com/encyclopedia/defineterm.jhtml?term=clock&x=&y=) cycle. There will be hundreds of output nodes on a chip and will have different load capacitance and different node transition activity factor. Thus, we can write a generalized equation of total average dynamic power dissipation as follows:



where Ci represents total capacitance associated with each node (node i),  
i represents the node transition factor associated with each node, and  
Vi is the voltage at which the Ci will charge. Hence the quantity in parenthesis represents the total charge drawn from the power supply during each transition.

From equation 3 we can easily interpret that by reducing one of the parameters in this equation dynamic power dissipation can be somewhat minimized. Power is always dissipated in CMOS circuit when there is switching at the output node. You can always reduce the power by reducing the operating frequency but due to continuous demand of increasing the speed of data rate in digital systems this method will not give the useful results. α, the node transition activity factor, is a statistical parameter and is data rate dependent and defines the probability of the gate's output to make logic transition during one clock cycle. Only we can predict and can make the rough estimate of its value. The remaining parameters are supply voltage VDD and the output load capacitance CL which are discussed below.

Voltage scaling  
It is obvious from the equation 2 that power dissipation can be minimized by reducing the supply voltage VDD. Although reduction in the supply voltage minimizes the dynamic power dissipation, the trade-off will be an increase in delay. This can be observed by looking at equations 4 and 5 for the propagation delay of a CMOS inverter:



We consider a metric the energy-delay product. The smaller energy\*delay value employs a lower energy solution at the same level of performance, and hence a more energy-efficient design as depicted in Figure 4.

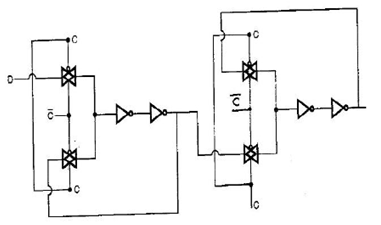


Figure showing conventional d flip flop implementation

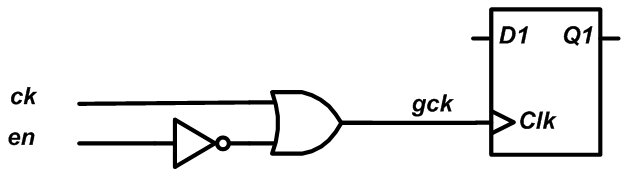


Figure shows insertion of gated clock to flipflop block

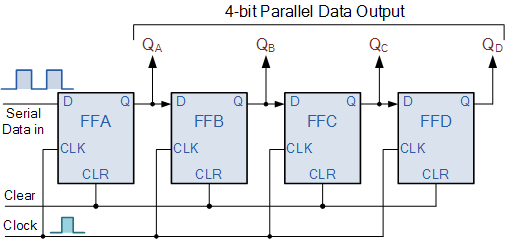


Figure showing register block

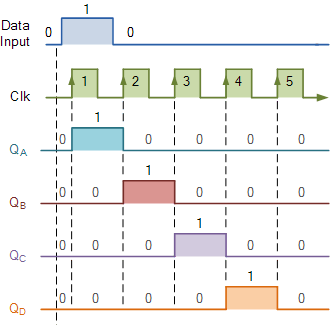
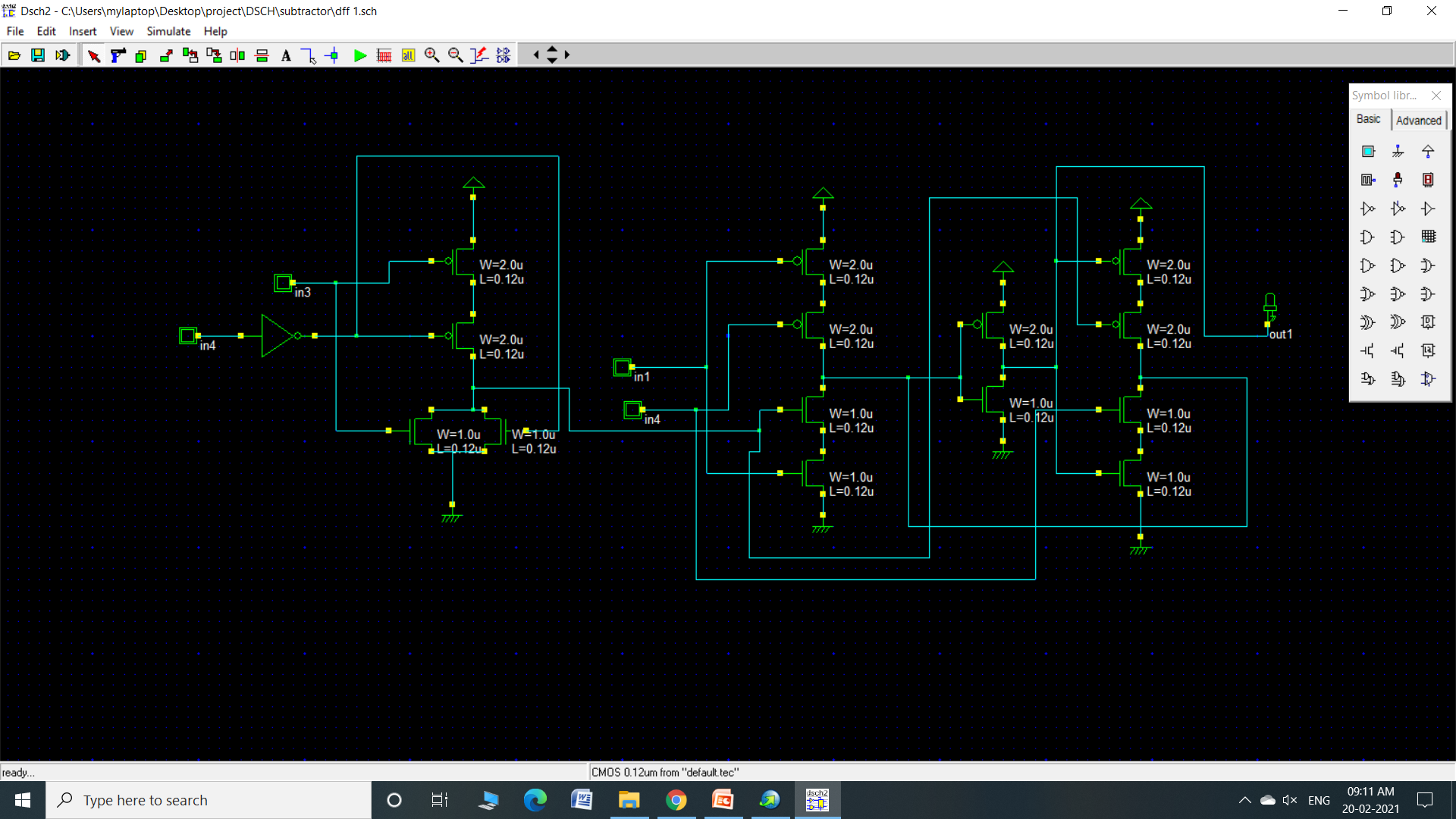
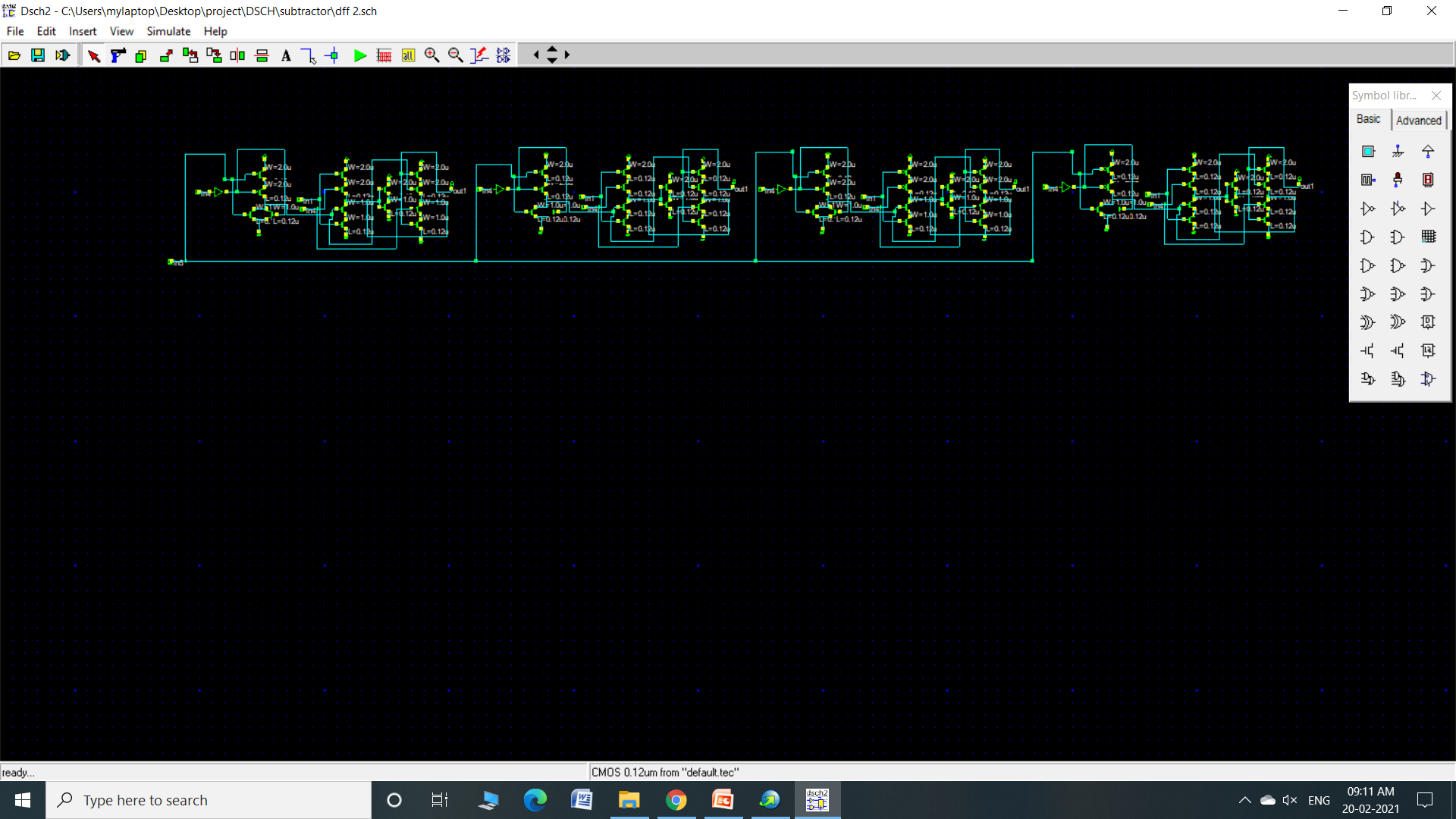


Figure showing register data transfer

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Implementation of flipflop model on dsch

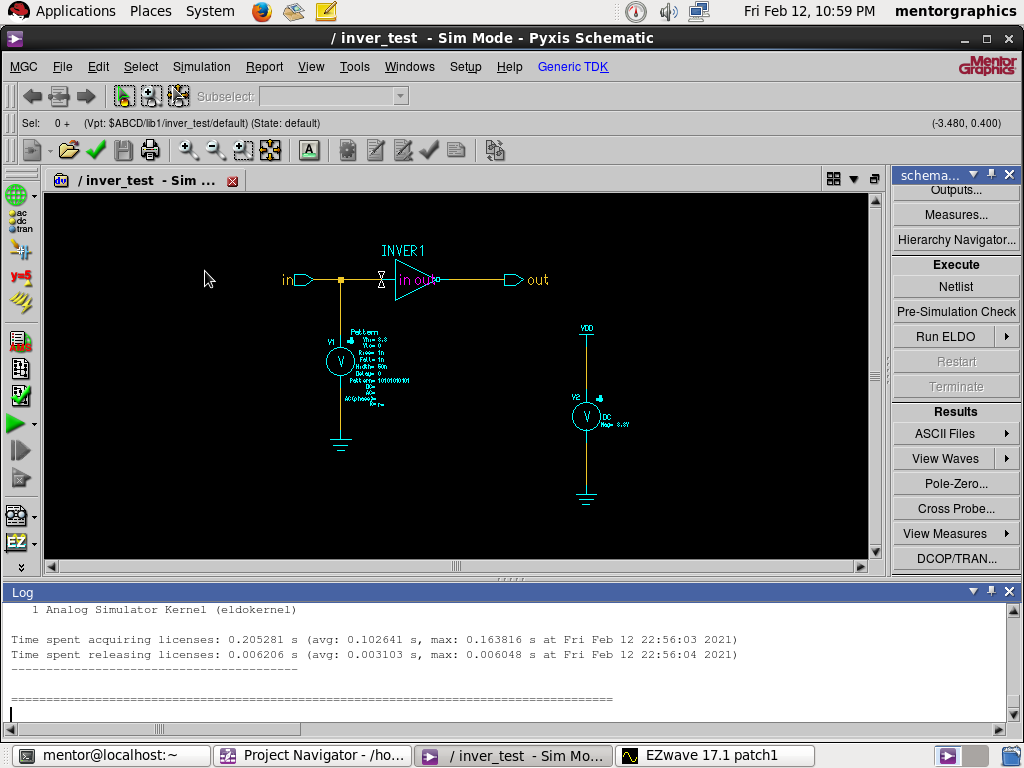
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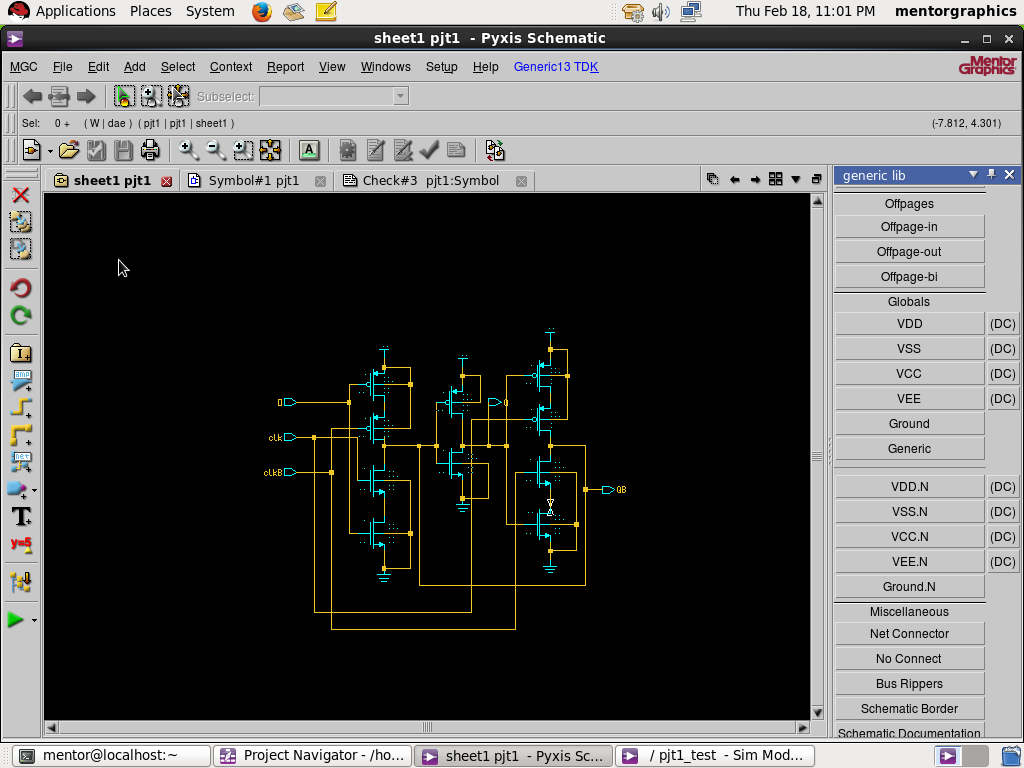
Implementation of register with d flipflops on dsch

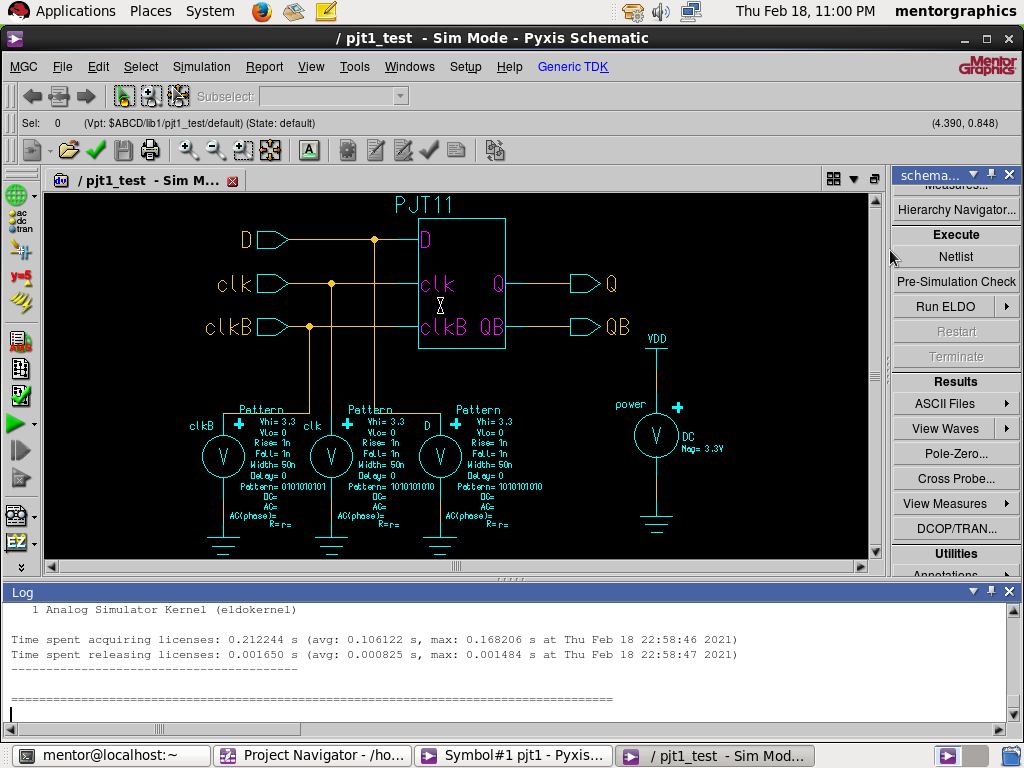
**Results on mentor graphics**

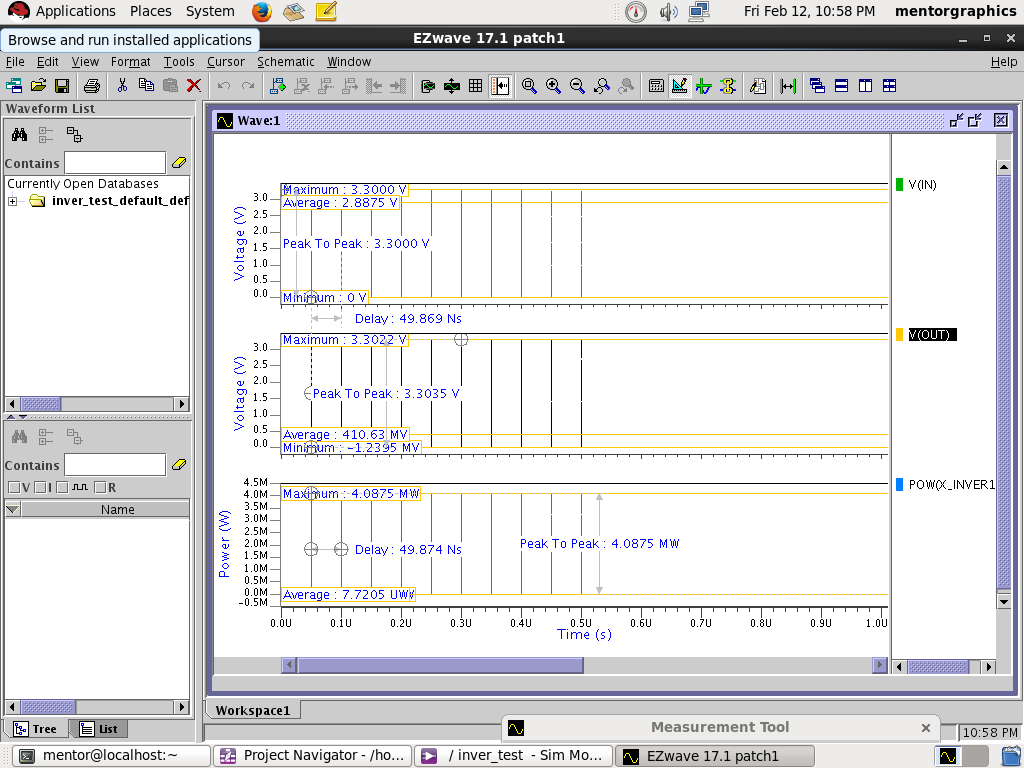
**Average power consumption of unmodified D flip flop**

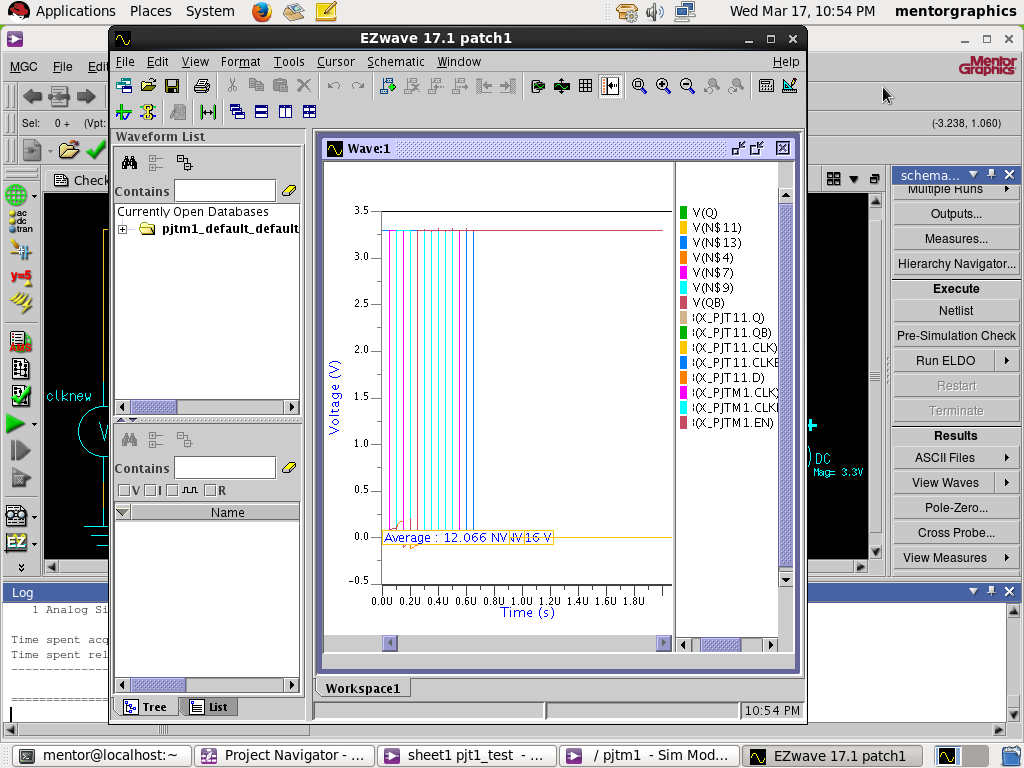
D flip flop without gated clock circuit is implemented on mentor graphics and power consumption is noted which will be later compared with gated clock D flip flop. Average power consumption of circuit is 7.72 micro watts. This circuit will further be implemented on unmodified PISO circuit



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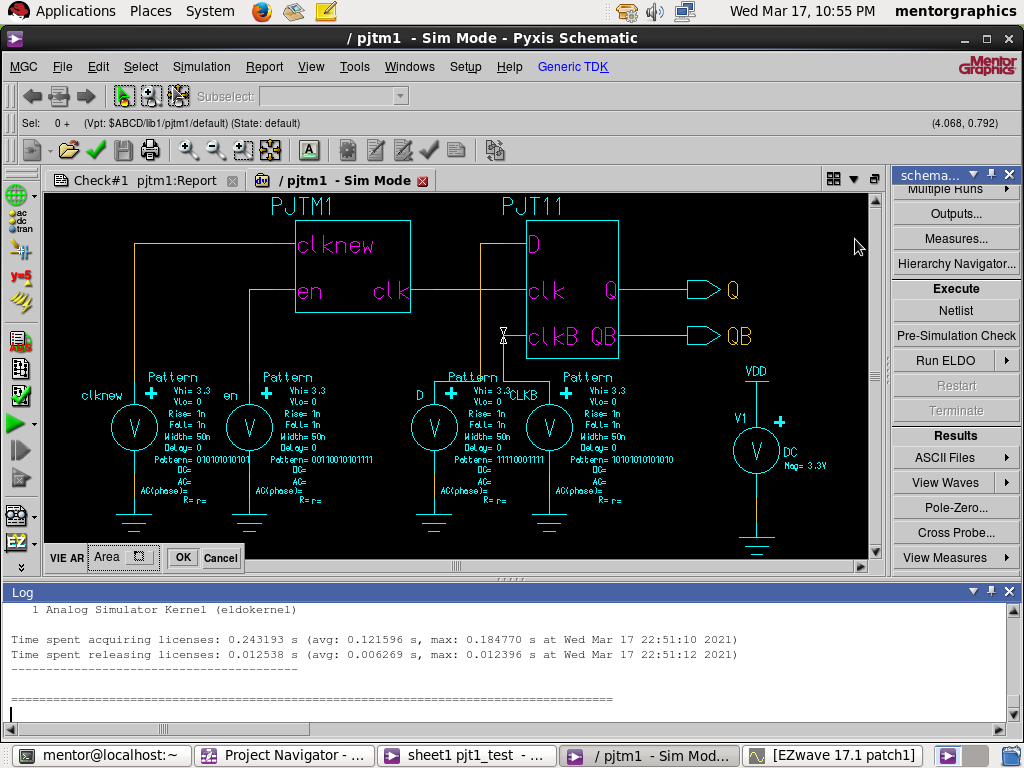
****

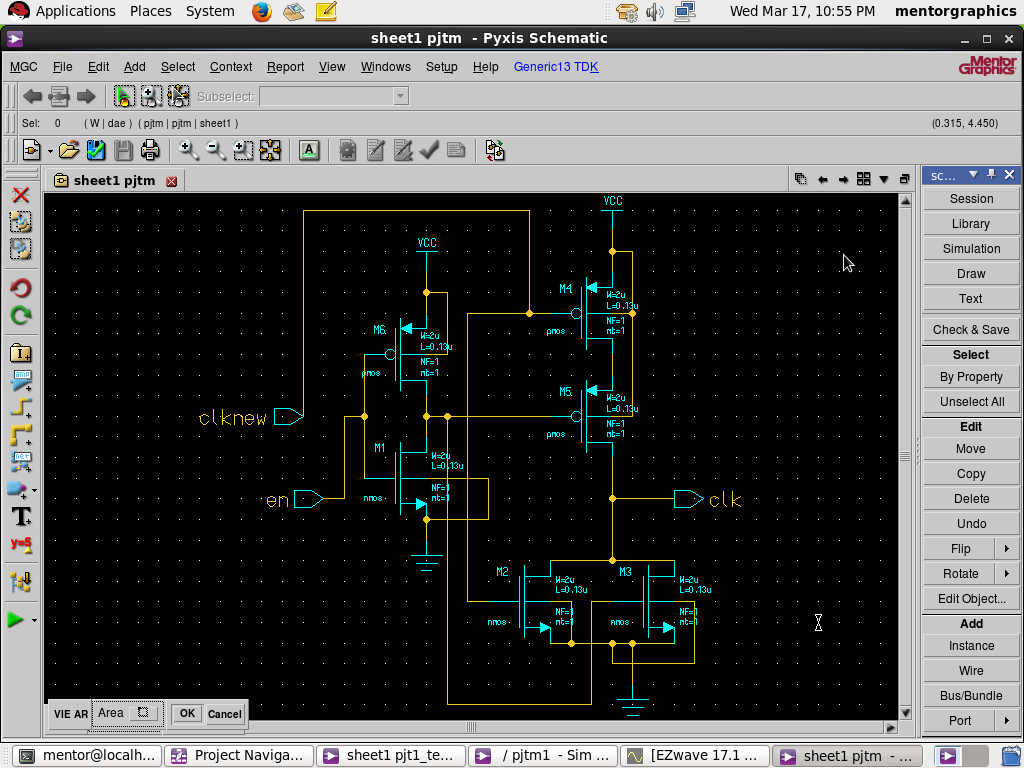
****

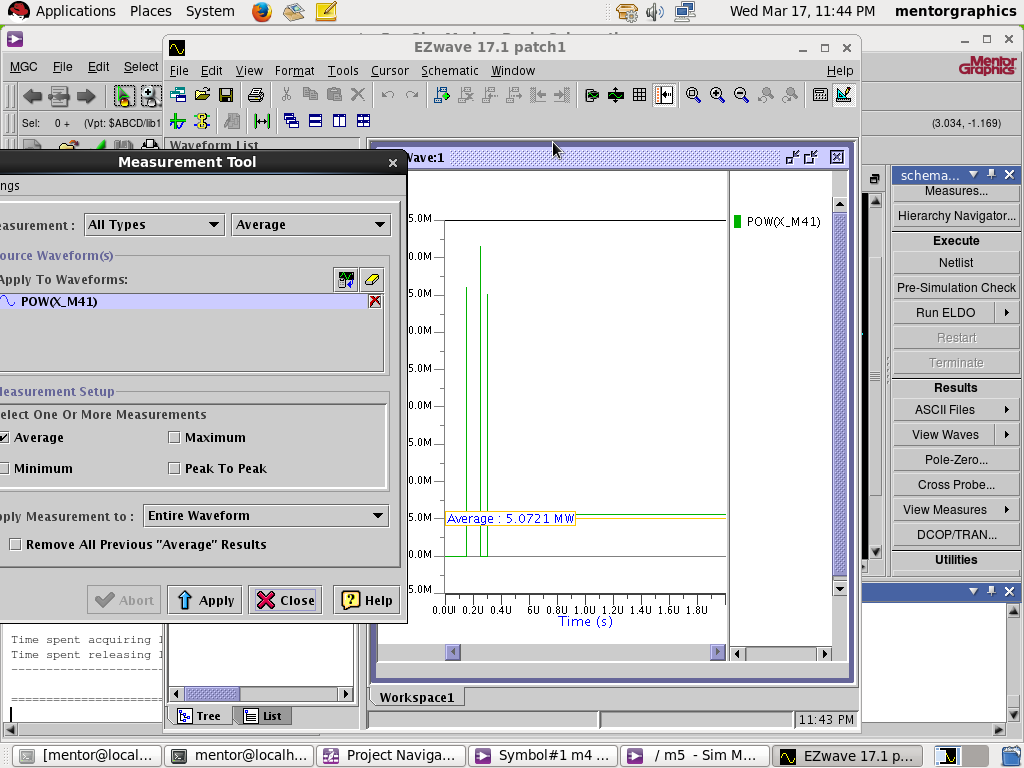
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**Average power consumption of modified D flip flop**

Figure 2 shows power consumption of modified circuit with gated flip flop circuit and average power is estimated to be 12.06 nw. This shows that the power consumption of modified one is less than previous circuit. This circuit will be later implemented on PISO circuit to calculate power consumed on real time application

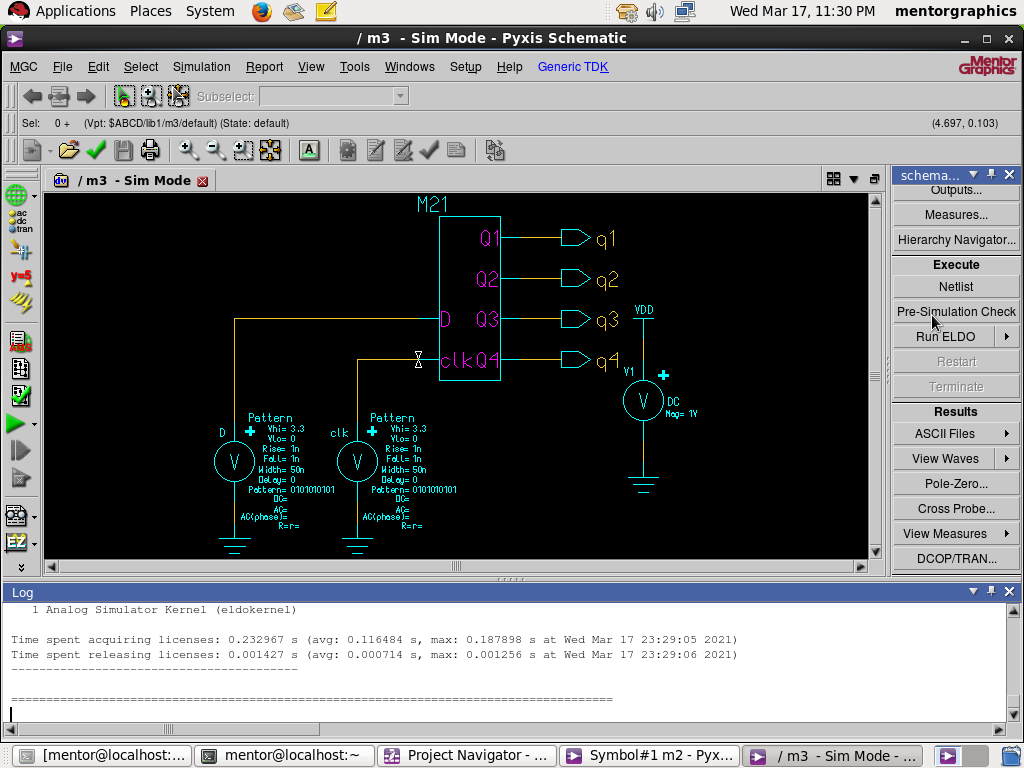
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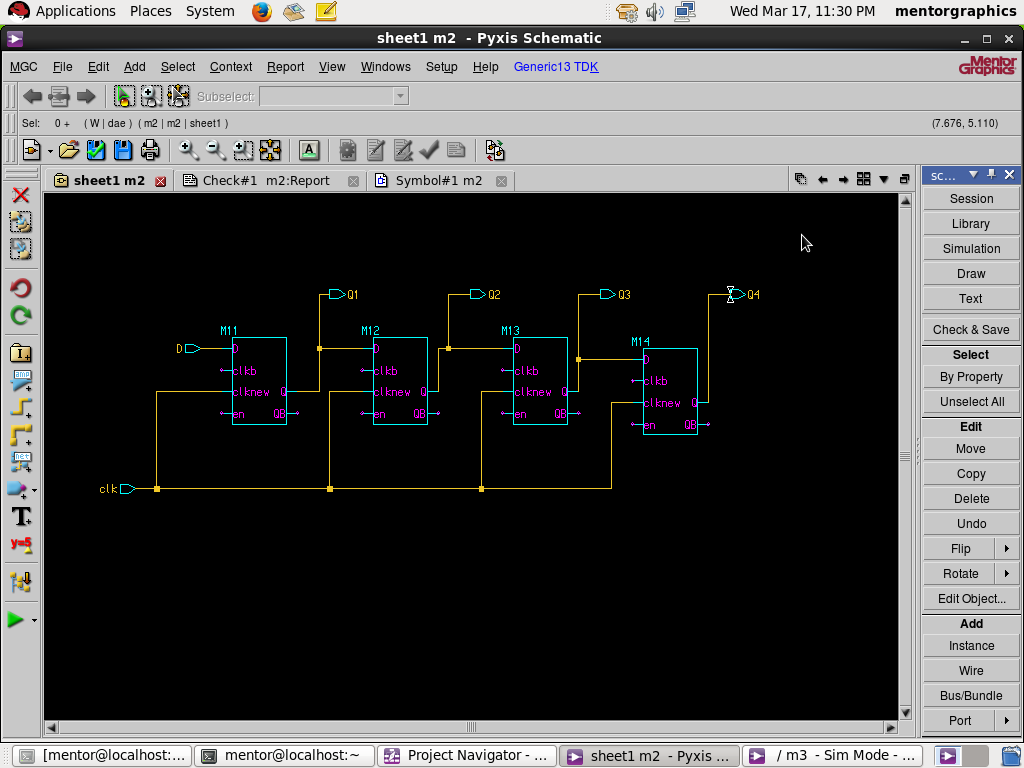
****

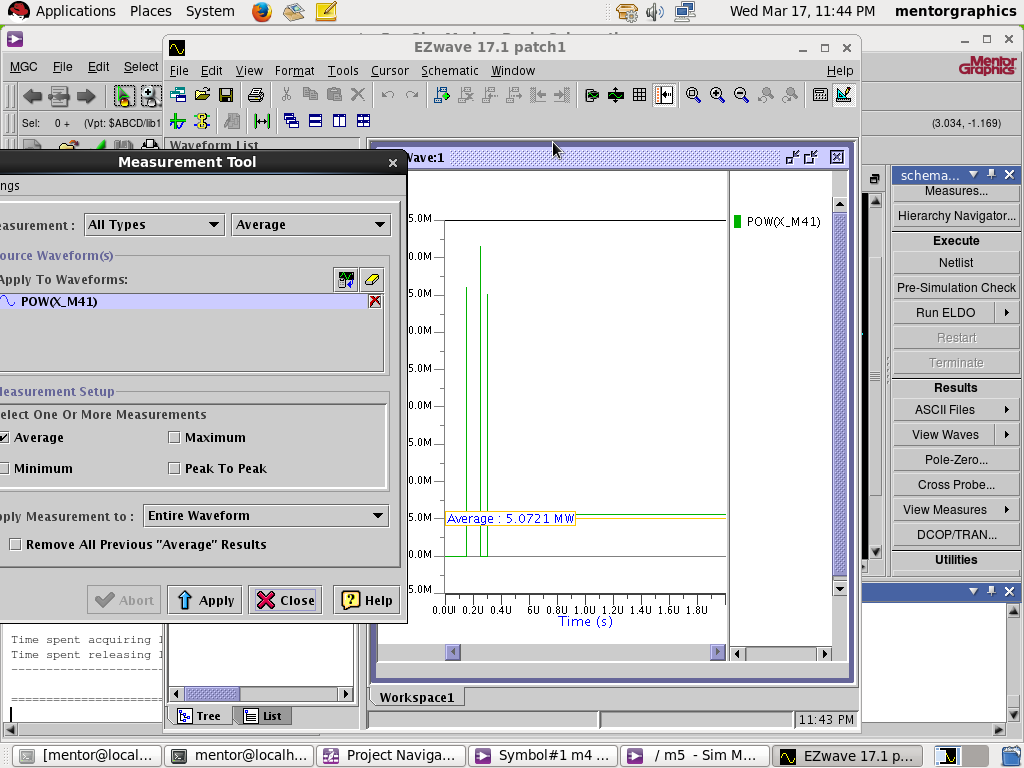
****

**Average power consumption of unmodified PISO circuit**

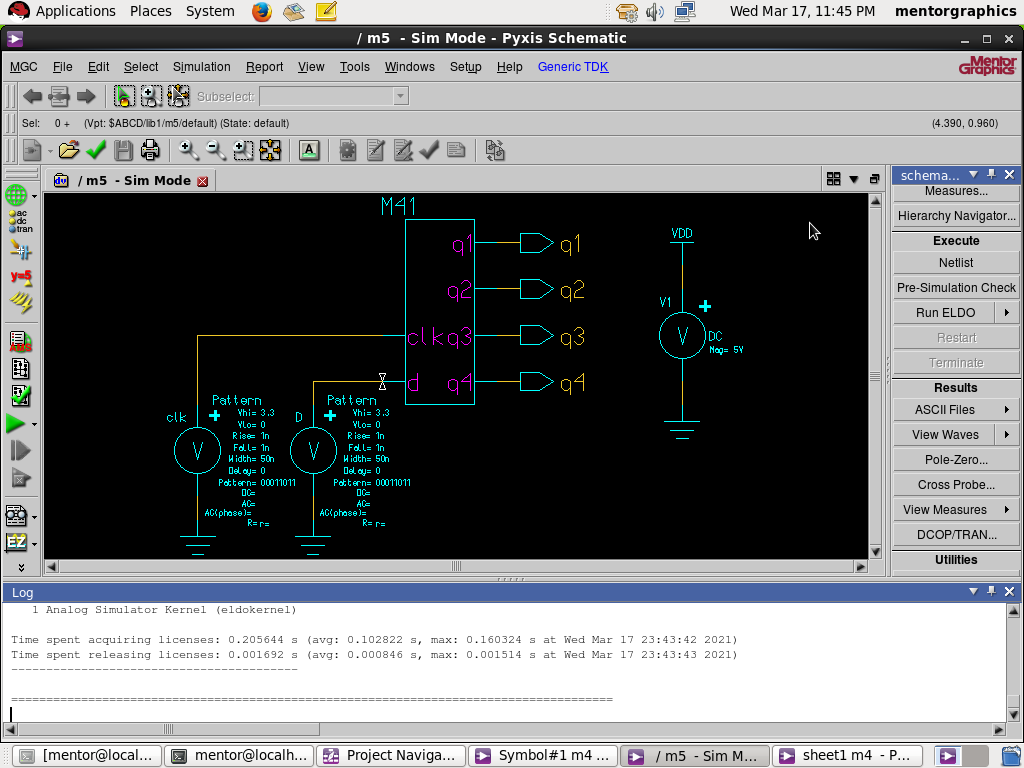
The D flip flop implemented previously will get converted to symbol on mentor graphics and used multiple times of memory element like PISO and average power will be calculated and compared with respect to modified circuit and the above circuit consumes 3.07mw

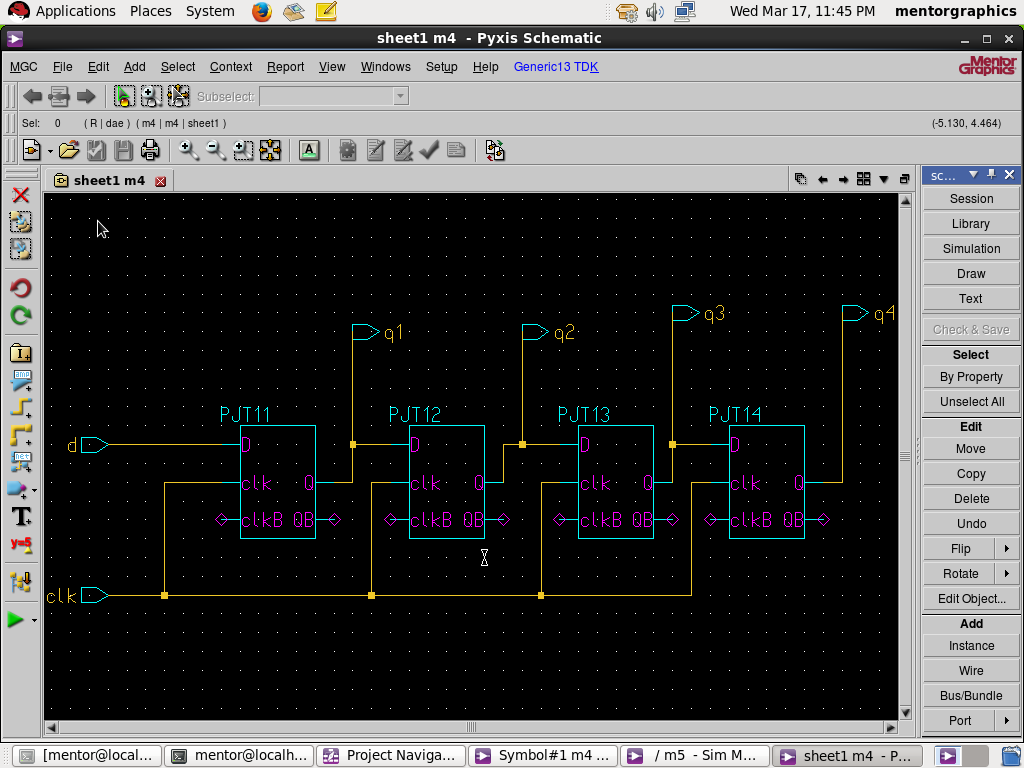
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**Average power consumption of modified PISO circuit**

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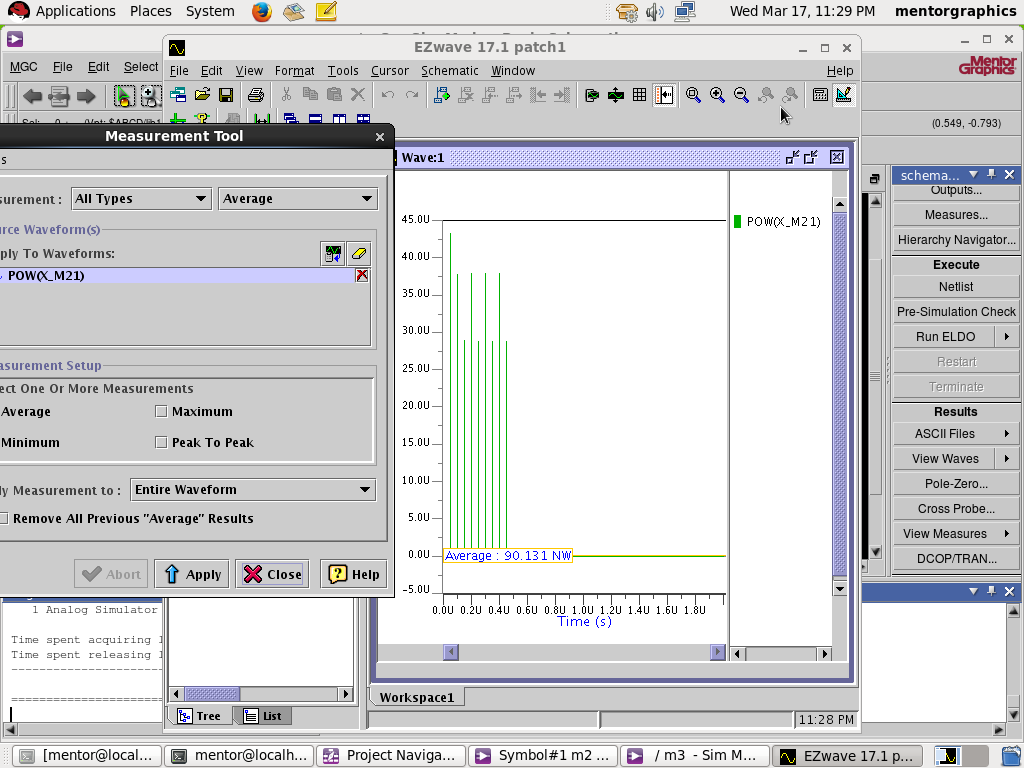
****

Figure 4 shows implementation of gated flip flop implemented PISO circuit and the results show that it consumes 90.1nw which is relatively less than unmodified circuit and is proven to be much reliable than original circuit since high power consumption reduces lifespan of devices

**Discussion of resuts**

In order to overcome the delay enlargement exhibited in previous clock-gated edge-triggered flip-flops, the idea of clock-gating a pulse-triggered flip-flop was adopted and implemented by using the best performed clock-gating scheme found out above. Delay and power measurements shown that the delay was not affected for our proposal and that the power reduction is more aggressive for a pulsetriggered flip-flop than for other schemes.

**Limitations**

By implementing this technique circuit could get some glitches in the gated clock if clock gating was not done properly. Which could cause severe problems. Improper control of the gating signal could result in big functional problems. Clock skew is greater between gated and un gated clocks. Overhead in design, verification and silicon area.

**Future direction**

This technique reduces dynamic power of circuit. Another important strategy to reduce circuit power consumption is to vary the threshold voltage within components, depending on the mode in which those components are running. High threshold voltages when a device is on standby or turned off can minimize leakage current, which reduces static power consumption.

**Reference and Bibilography :**

[1] Xia W.Q.shui,X.Y and Yao, W.L “Dual-vth based double-edge explicit-pulseed level-converting flip-flop” in IEEE-International Conference on Electronics ,communications and control (ICECC),(2011) [2] Bhargavaram,D.and Pillai,M.,”low power dual edge triggered flipflop”. in Advance in Engineering,science and Management (ICAESM),International Conference on IEEE,(2012),63-67. [3] B. Kong, S. Kim, and Y. Jun, “Conditional capture flipflop for statistical power reduction,” IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001. [4] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, “Conditional pre charge techniques for power-efficient dualedge clocking,” in Proc. Int. Symp. Low-Power Electron. Design, Aug. 2002, pp. 56–59. [5] P. Zhao, T. Darwish, and M. Bayoumi, Highperformance and low power conditional discharge flip-flop,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May 2004. [6] M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, “A low-power static dual edge triggered flip-flop using an outputcontrolled discharge configuration,” in Proc. IEEE Int. Symp. Circuits Syst., May 2005, pp. 2429–2432. [7] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, “Low power pulse triggered flip-flop design with conditional pulse enhancement scheme,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 361– 366, Feb. 2012. [8] Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme IEEE transactions on very large scale integration (VLSI) systems, vol. 22, no. 1, january 2014. [9] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, “Ultra low power clocking scheme using energy recovery and clock gating,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 33–44, Jan. 2009.

### The Arrangement of paragraph in a Chapter

Each topic Title in a chapter should be properly numbered for example: 2.1, 2.2 etc., (Bold and Upper case) where, the first digit represents the Chapter number, and second digit, the topic Title number.

Sub-topic titles, if any, may be indicated as 1.1.1,1.1.2, etc.( Bold and title case)

i.e .the representing the chapter, the second representing the topic title and the third representing the sub-topic title.

### Photographs and Tables:

The photographs and tables occurring in a chapter may be serially numbered as Fig: 1.1, 1.2 etc., along with suitable CAPTION where the first digit represents the chapter, the second digit represents figure number.

The photograph may be represented as: plate 1.1, 1.2 etc., the first representing chapter and the second representing the photograph number.

### Graphs:

The graph should clearly indicate the points which are used for drawing the curve or curves along with error bars. The axes ( X,Y and Z) should have CAPTIONS.

### Bibliography or References:

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